Nanometer-Scale III-V CMOS

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Abstract:

In the last few years, as Si electronics faces mounting difficulties to maintain its historical scaling path, transistors based on III-V compound semiconductors have emerged as a credible alternative. To get to this point, fundamental technical problems had to be solved though there are still many challenges that need to be addressed before the first non-Si CMOS technology becomes a reality. Among them, harnessing the outstanding electron transport properties of InGaAs, the leading n-channel material candidate, towards a high-performance nanoscale MOSFET has proven difficult: contact resistance, off-state characteristics, reliability and Si integration remain serious problems. Introducing a new material system is not the only challenge, scalability to sub-10 nm gate dimensions also demands a new 3D transistor geometry. InGaAs FinFETs, Trigate MOSFETs and Nanowire MOSFETs have all been demonstrated but their performance is still disappointing. To compound the challenge, a high-performance nanoscale p-type transistor is also required. Among III-Vs, InGaSb is the most promising candidate. Planar MOSFETs have been demonstrated but more advanced geometries remain elusive. This talk will review recent progress as well as challenges confronting III-V electronics for future CMOS logic applications.